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| 10/716,808 | 11/19/2003 | Brian Celella | SIE-0157 | 6766 |

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| EXAMINER | |
|---|---|
| VIGUSHIN, JOHN B | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2841 | |

DATE MAILED: 05/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

HA

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/716,808 | CELELLA ET AL. | |
| | Examiner | Art Unit | |
| | John B. Vigushin | 2841 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *08 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9* is/are allowed.

6)☒ Claim(s) *1 and 11-14* is/are rejected.

7)☒ Claim(s) *2-8 and 10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. The present Office Action is responsive to Applicant's amended response filed February 08, 2006. The Examiner acknowledges the amendments to Claims 1-5, 9 and 14. Claims 1-14 remain pending in the instant amended Application.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1 and 11-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Weatherley (US 6,333,472 B1).

As to Claim 1, Weatherley discloses a printed circuit board 1 comprising: first plated through-holes 2 for receiving a first connecting component (Fig. 1; col.3: 54-59); second plated through-holes 3 for receiving a second connecting component (Fig. 1; col.3: 60-63); a signal carrying trace 5 for transmitting a signal from one of the first plated through-holes 2 (marked t1 in Fig. 3-1) to one of the second plated through-holes 3 (marked T1 in Fig. 3-1; col.4: 30-35); a trace 6 (inherently, trace 6 is a phase delay control trace) in electrical connection with plated through-hole t1, the phase delay control trace 6 inherently affecting delay of the signal from first plated through-hole t1 to

second plated through hole T1 (Fig. 3-1; col.3: 26-30 and col.4: 30-36). *Examiner's Note*: While Weatherley does not explain how the "loop" configurations--that branch from a single track (5, for example, in Fig. 3-1) into two tracks 6 then converge back into a single track 5--perform the crosstalk reduction, the Weatherley configuration nevertheless appears to be structurally and functionally the same as that in Applicant's disclosure (see disclosure Fig. 6 and Specification, p.6, paragraph [0026]), wherein Weatherley's trace 6 (Fig. 3-1) functions as the "redundant" trace analogous to the redundant trace 60 in Applicant's Fig. 6 and therefore inherently performs the same phase delay control function as does Applicant's redundant trace 60 for reducing crosstalk. The structure of signal trace 5 as disclosed in Weatherley has the property of an effective parallel resistance $R_{eff}$ determined by the resistances $R_5$ and $R_6$ inherent in each of parallel conductors 5 and 6, respectively, the effective parallel resistance $R_{eff}$ being less than that of $R_5$, since $R_5$ of signal trace 5 exhibits the smaller of the two parallel resistances $R_5$ and $R_6$, from circuit theory--$R_{eff} \equiv R_5 \| R_6 = (R_5 \times R_6) \div (R_5 + R_6)$--(note that conductor 5 is **shorter in length L** than phase control trace conductor 6, and recall that a conductor resistance $R = \rho L/A$, where $\rho$ is resistivity of the conductor material, L is the conductor length and A is the conductor's cross-sectional area. Since the portion of conductor 5 parallel to conductor 6 is shorter than conductor 6, then $R_5 < R_6$ and $R_{eff} < R_5$). Since the signal transmitted from hole t1 to hole T1 in Fig. 3-1 sees an effective resistance $R_{eff}$--at the point of signal line bifurcation into parallel lines 5 and 6--that is less than the resistance $R_5$ of signal trace 5, then the properties inherently associated with a signal in conductor 5 seeing such an $R_{eff}$ lower than signal trace 5

flow naturally from the structure; i.e., trace 6, the phase delay control trace 6 is effectively configured--in Weatherley, the configuration of trace 6 consists in its being made parallel to signal trace 5--to inherently shift the phase of compensating crosstalk. The shift in phase of compensating crosstalk is a property of the above-described bifurcated signal line structure in Weatherley, regardless of the fact that Weatherley does not see fit to explicitly enunciate this crosstalk reduction effect. Nevertheless, Weatherley established the above-described wiring structure, with the inherent phase shifting effect, as claimed by the Applicant, for reducing the crosstalk by phase delay control in conjunction with the disclosed crosstalk-reducing capacitive coupling.

As to Claim 11, Weatherley further discloses the first connecting component is an outlet (col.3: 54-59).

As to Claim 12, Weatherley further discloses the second connecting component is a wire termination block (col.3: 60-65).

As to Claim 13, Weatherley further discloses, in Fig. 3-1, a crosstalk magnitude control trace 8 in electrical connection with said one of the first plated through holes--i.e., through hole t1 (col.4: 38-41)--the crosstalk magnitude control trace being reactively (capacitively) coupled with another trace (col.2: 6-22)--i.e., trace 22 in Fig. 3-5 which is the reverse side of the Fig. 3-1 board (col.4: 59-64)--to control crosstalk magnitude (col.5: 17-25).

As to Claim 14, Weatherley discloses: a first component for connection with a first cable (col.3: 54-59 and col.5: 30-42); a second component for connection with a second cable (col.3: 60-64 and col.5: 30-42); a printed circuit board 1 (Fig. 2) providing

crosstalk compensation, the printed circuit board 1 including: first plated through-holes 2 for receiving a first connecting component (Fig. 1; col.3: 54-59); second plated through-holes 3 for receiving a second connecting component (Fig. 1; col.3: 60-63); a signal carrying trace 5 for transmitting a signal from one of the first plated through-holes 2 (marked t1 in Fig. 3-1) to one of the second plated through-holes 3 (marked T1 in Fig. 3-1; col.4: 30-35); a trace 6 (inherently, trace 6 is a phase delay control trace) in electrical connection with plated through-hole t1, the phase delay control trace 6 inherently affecting delay of the signal from first plated through-hole t1 to second plated through hole T1 (Fig. 3-1; col.3: 26-30 and col.4: 30-36). *Examiner's Note*: While Weatherley does not explain how the "loop" configurations--that branch from a single track (5, for example, in Fig. 3-1) into two tracks 6 then converge back into a single track 5--perform the crosstalk reduction, the Weatherley configuration nevertheless appears to be structurally and functionally the same as that in Applicant's disclosure (see disclosure Fig. 6 and Specification, p.6, paragraph [0026]), wherein Weatherley's trace 6 (Fig. 3-1) functions as the "redundant" trace analogous to the redundant trace 60 in Applicant's Fig. 6 and therefore inherently performs the same phase delay control function as does Applicant's redundant trace 60 for reducing crosstalk. The structure of signal trace 5 as disclosed in Weatherley has the property of an effective parallel resistance $R_{eff}$ determined by the resistances $R_5$ and $R_6$ inherent in each of parallel conductors 5 and 6, respectively, the effective parallel resistance $R_{eff}$ being less than that of $R_5$, since $R_5$ of signal trace 5 exhibits the smaller of the two parallel resistances $R_5$ and $R_6$, from circuit theory--$R_{eff} \equiv R_5 \| R_6 = (R_5 \times R_6) \div (R_5 + R_6)$--(note that conductor 5 is **shorter in**

**length L** than phase control trace conductor 6, and recall that a conductor resistance R = $\rho$L/A, where $\rho$ is resistivity of the conductor material, L is the conductor length and A is the conductor's cross-sectional area. Since the portion of conductor 5 parallel to conductor 6 is shorter than conductor 6, then $R_5 < R_6$ and $R_{eff} < R_5$). Since the signal transmitted from hole t1 to hole T1 in Fig. 3-1 sees an effective resistance $R_{eff}$--at the point of signal line bifurcation into parallel lines 5 and 6--that is less than the resistance $R_5$ of signal trace 5, then the properties inherently associated with a signal in conductor 5 seeing such an $R_{eff}$ lower than signal trace 5 flow naturally from the structure; i.e., trace 6, the phase delay control trace 6 is effectively configured--in Weatherley, the configuration of trace 6 consists in its being made parallel to signal trace 5--to inherently shift the phase of compensating crosstalk. The shift in phase of compensating crosstalk is a property of the above-described bifurcated signal line structure in Weatherley, regardless of the fact that Weatherley does not see fit to explicitly enunciate this crosstalk reduction effect. Nevertheless, Weatherley established the above-described wiring structure, with the inherent phase shifting effect, as claimed by the Applicant, for reducing the crosstalk by phase delay control in conjunction with the disclosed crosstalk-reducing capacitive coupling.

***Allowable Subject Matter***

4. Claim 9 has been allowed.

5. Claims 2-8 and 10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The following is a statement of reasons for the indication of allowable subject matter:

As to Claim 2, patentability resides in the limitation wherein *the phase delay control trace and the signal carrying trace are the same single trace*, in combination with the other limitations of the claim.

As to Claim 3, patentability resides in the limitation wherein *the phase delay control trace is made from a material having a conductivity different than the conductivity of a material of other traces on the printed circuit board*, in combination with the other limitations of the claim.

As to Claim 4, patentability resides in the limitation wherein *the phase delay control trace includes multiple redundant phase delay control traces in order to provide increased conductivity*, in combination with the other limitations of the claim. *Examiner's Note*: Weatherley discloses only one phase delay control trace 6 which forms the bifurcation in the signal trace 5 (Fig. 3-1).

As to Claim 5, patentability resides in the limitation wherein *the phase delay control trace includes an increased cross-sectional dimension relative to other traces on the printed circuit board in order to provide the increased conductivity*, in combination with the other limitations of the claim.

As to Claim 6, patentability resides in the limitation wherein *the phase delay control trace is an isolated dead end trace separate from signal carrying trace, the dead, the dead end trace isolated to avoid reactive coupling with other traces*, in combination with the other limitations of the claim. *Examiner's Note*: Weatherley does not disclose such an isolated trace, since dead end traces such as loop traces 7 and 8, for example (Fig. 3-1), are intentionally positioned in the layout to reactively (i.e., capacitively) couple with traces 22 (Fig. 3-5) and 15 (Fig. 3-3), respectively.

As to Claims 7-8 and 10, patentability resides in the limitation wherein *the phase delay control trace includes a first phase delay control trace and a second phase delay control trace*, in combination with the other limitations of the broadest claim, Claim 7. *Examiner's Note*: Weatherley does not teach that phase delay control trace includes first and second phase delay control traces.

As to Claim 9, patentability resides in the limitation wherein *the signal carrying trace has an increased thickness in order to affect the phase delay of the signal from said one of said first plated through holes to said one of said second plated through holes*, in combination with the other limitations of the claim.

### *Response to Arguments*

7. Applicant's arguments filed February 08, 2006 have been fully considered but they are not persuasive with respect to the Examiner's rejection of base Claims 1 and 14 over Weatherley (US 6,333,472 B1).

(i) The Examiner agrees with the Applicant that the traces are overlapped to perform crosstalk reduction by capacitive coupling. However, the Examiner notes that, in addition to the capacitive coupling, there is disclosed a bifurcation of signal trace 5 into traces 5 and 6, as well as the bifurcation of signal trace 10 into traces 10 and 11, resulting in capacitively coupled wiring structures that are not like the other capacitively coupled loops in the compensation board of Weatherley. In particular, trace 5 carries the signal from through-hole t1 to through-hole T1 and the bifurcation caused by trace 6 creates an effective parallel trace resistance on the signal line formed by signal trace 5 and control trace 6, which effectively reduces the resistance of signal trace 5 as seen by the signal as it approaches the point of bifurcation, the control trace 6 thereby functioning as a phase delay control trace configured to shift the phase of compensating crosstalk by forming a parallel resistance path with signal trace 5, the phase shift of the compensating crosstalk being the *inherent* result of the bifurcated structure disclosed in Weatherley (see Fig. 3-1). Even though Weatherley does not point out this natural effect of the parallel traces 5 and 6 in the layout, the parallel and bifurcated structure, nevertheless, is clearly disclosed as part of the overall circuit layout and the electrical properties of the wiring structure flow naturally from the electrical effects inherent in the wiring structure. Accordingly, the Examiner respectfully disagrees with the Applicant and takes the position that Weatherley does, in fact, teach a circuit layout of the compensation board comprising "the phase delay control trace [6] configured to shift the phase of compensating crosstalk" in addition to crosstalk reduction by capacitive

coupling. This position taken by the Examiner is explained in greater detail in the rejections of amended base Claims 1 and 14, set forth above.

(ii) Applicant's arguments on p.7 of Applicant's instant Amendment, filed February 08, 2006, with respect to the Examiner's rejection of Claims 1-3, 5 and 13 over Winings (US 6,250,968 B1) have been fully considered and are persuasive. The wiring structure disclosed by Winings is, in fact, strictly for the purpose of producing compensating crosstalk using reactive coupling only (col.5: 41-51; col.6: 19-56); as pointed out by the Applicant, no "phase delay control trace configured to shift the phase of compensating crosstalk" is taught or fairly suggested. Accordingly, the rejection of Claims 1-3, 5 and 13 over Winings has been withdrawn.

(iii) The Examiner has reconsidered the rejections of Claims 2-8 and 10 over Weatherley, both in light of Applicant's amendments to Claims 2-5 as well as the Examiner's own re-evaluation of Weatherley vis-à-vis Claims 4, 6 and 7. The Examiner has added notes to the reasons for allowance of Claims 4, 6 and 7 (see section 6, above) explaining how the Examiner now sees the features of those claims that patentably distinguish over Weatherley.

(iv) Claims 11-13 remain rejected over Weatherley, in addition to amended Claims 1 and 14. However, the Examiner has substantially changed the rejection of Claim 13 to replace the rejection in the previous Office Action of November 08, 2005 (section 5, p.9) with a more accurate one that correctly identifies a "crosstalk magnitude control trace" which is taught by Weatherley as "reactively coupled with another trace to control crosstalk magnitude".

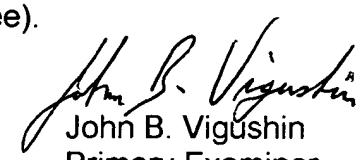
***Conclusion***

8. Although Applicant amended base Claims 1 and 14, the corrective and substantial change in the rejection of Claim 13, as initiated by the Examiner, makes the present Office Action NON-FINAL.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 571-272-1936. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



John B. Vigushin
Primary Examiner
Art Unit 2841

jbv
April 25, 2006